ADVANCED PACKAGING AND INTEGRATION TECHNOLOGIES FOR MICROSENSORS

KULITE SEMICONDUCTOR PRODUCTS, INC.

Principal Investigator: Dr. A.D. Kurtz

Researcher: A. A. Ned

REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

1. AGENCY USE ONLY (Leave blank)	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	8/12/94	Phase I Final Report Feb.-July 1994

4. TITLE AND SUBTITLE
Advanced Packaging & Integration Technologies for Microsensors Final Report

5. FUNDING NUMBERS

6. AUTHOR(S)
A. A. Ned and A. D. Kurtz

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
Kulite Semiconductor Products, Inc.
One Willow Tree Rd.
Leonia, NJ 07605

8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)
U. S. Army Research Lab
Fort Monmouth, Site Contracts Branch
Fort Monmouth, NJ 07703-5601

10. SPONSORING/MONITORING AGENCY REPORT NUMBER

11. SUPPLEMENTARY NOTES

12a. DISTRIBUTION/AVAILABILITY STATEMENT
Approved for public release, distribution unlimited.

12b. DISTRIBUTION CODE

13. ABSTRACT *(Maximum 200 words)*

Advanced microfabrication processes have been developed for producing a hermetic cover wafer with low resistance dielectrically isolated through-wafer interconnects.The feasibility of manufacturing encapsulated pressure sensors, utilizing the cover-wafer approach, has been demonstrated. Such pressure sensors represent a new generation of environmentally protected, cost effective devices. The accomplishments of Phase I include the following: a. The study of conversion of single crystal silicon into porous silicon. b. The study of conversion of porous silicon into oxide. c. Process for producing through-wafer interconnects has been established. d. The stresses in the cover wafer have been investigated, which enabled the fabricaton of flat cover-wafers. e. The surface and cross-sectional morphology of the cover wafer was investigated. f. Hermeticity and dielectric isolation of the oxidized rings was verified. g. Sensors compatible with the cover-wafer approach were fabricated and tested. The new generation of sensors was designed.

14. SUBJECT TERMS			15. NUMBER OF PAGES
			16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
Unclassified	Unclassified	Unclassified	UL

INTRODUCTION

Piezoresistive pressure sensors have been utilized by the U.S. Army in various military applications. Sensors are used in rotary wing aircraft, such as the Cobra and Apache helicopters, to monitor oil, engine and hydraulic pressures. Military diesel engine vehicles require pressure sensors to measure fuel, oil and engine coolants. In tanks, such as the M1, sensors are utilized for engine diagnostics and hydraulic turret control. Pressure sensors are applied to monitor the system operation conditions in missiles and missile launchers. In landing craft vehicles microsensors are employed to monitor pressures in the oil, fuel and across filters. For many of the above applications, it would be beneficial to have sensors which could operate at high temperatures and in hostile environments.

SCIENTIFIC AND TECHNOLOGICAL BACKGROUND

Hermetic sealing of semiconductor devices is well known in the art. Modern process technology is replete with externally fabricated covers of non-silicon materials, usually ceramics, which hermetically seal a semiconductor device.

The present research, however, relates to a novel method for providing a hermetically sealed semiconductor device which utilizes a micromachined integral silicon structure which not only effects a hermetic seal but can be fabricated in wafer form using basically standard semiconductor fabrication technology. In addition, by using a silicon wafer as the starting material, the resulting hermetically sealed structure can be fabricated

with much lower internal stresses than hermetically sealed prior art devices. This is because the prior art methods use materials for the cover wafers which are different from the material used for the device wafer. As such, none of these materials can match the thermal expansion coefficients of silicon as well as silicon itself. Furthermore, all other materials used have very low thermal conductivities. The use of silicon with its high thermal conductivity, allows much greater heat dissipation[1].

In the present research, the contact areas are already present in the starting material and during the fabrication process, the bulk material of the starting material is isolated from the portion of the starting material that will form the contact areas. This isolation is achieved by using photolithographic techniques to form a multiplicity of isolations in one process. Moreover, the use of photolithography provides a much superior method for controlling both the area of the contact regions and their respective isolations. The use of photolithography allows the contact regions to be configured, as desired, into any shape such as a circle, square, rectangle or even a ring or a spiral.

In contrast, present technology use the formation of holes through the insulating material and the filling of the holes with conductive material. Forming holes in a wafer of insulating materials is much more difficult than creating a thin ring of isolated material. Additionally, fabricating the hole-filling material requires a deposition step which results in inconsistent adhesion to the insulator used as a cover. Since the feedthroughs, in the present work, will be made of silicon, they can be joined to the underlying wafer by many methods such as fusion bonding of silicon to silicon, eutectic bonding by metalizing either the underlying wafer or the cover wafer etc.

The proposed innovation presents a significant advance in the area of sensor technology. A structure is suggested in which a piezoresistive pressure sensor wafer is bonded to a cover wafer. The cover wafer contains through-wafer interconnects, which provide electrical contact to the piezoresistor network, as well as hermetically sealing the sensor wafer. Pressure can thus be applied from the backside. The cover-wafer can be mounted directly to a board or header, without the use of external leads, either by using solder bump or eutectic bonding. This approach allows part of the sensor packaging (e.g. sealing form the environment) to be done at the wafer level as a batch process thus increasing reliability and reducing costs.

The work in Phase I has demonstrated the feasibility of the above approach. All of the conceptual problems associated with the proposed approach have been solved. We have shown that we can construct a cover wafer with dielectrically-isolated, hermetic feed-throughs suitable for bonding to another wafer. In order to accomplish this result, the technology/processes was developed for the fabrication of an encapsulated sensor with an extended contacts cover wafer. The research was divided into a number of sub tasks:

Section I) The study of the conversion of single crystal silicon into porous silicon and its dependance on process parameters. Of particular importance was the establishment of methods to control the degree of porosity, the pore size and the interpore spacing. In addition, it was necessary to determine conditions to enable one to etch through a complete wafer.

Section II) The study of the conditions for the conversion of porous silicon into oxide as a function of time, temperature, porosity, and pore size in order to

produce oxidized vias (rings) through the entire wafer.

Section III) The study of the stresses produced by the oxidation of the porous material to enable the fabrication of flat, effectively stress-free, wafers for further processing.

Section IV) The investigation of surface and through-wafer morphologies in order to provide for complete understanding of our processing and its effects on the cover-wafers.

Section V) The study of methods for fabrication of sensors, compatible with the extended contacts cover-wafer.

Section VI) The study of electrical isolation (contact to contact and/or to field) and hermeticity of the cover wafer.

DETAILED TASK DISCRIPTION

Section I: Conversion of Single Crystal Si into Porous Si

A. Starting Material

In order to limit the amount of added resistance due to the extended contacts a very low resistivity Si was selected [.003ohm-cm, (110) P-type silicon]. The added resistance of the contacts, based on the geometrical layout of the masks, was calculated to be on the order of .5 ohms. This silicon was found appropriate for the feasibility study and was utilized for the fabrication of the cover-wafers.

B. Masking for Anodization

1. Silicon Nitride Mask.

Thermally deposited silicon nitride (Si_3N_4) was the first masking film to be evaluated. Using a mask with circular openings enabled us to define patterns in the

silicon nitride film. During the anodization, the silicon nitride survived in 20% HF for 40 minutes which was found to be not sufficient to withstand anodization of silicon through the wafer.

2. Platinum Mask

1,000Å of Pt was sputtered, to be used as the masking material for anodization. Platinum is inert in HF and can be defined very easily using an aqua regia type etch. Pt survived for up to 4 hours in HF, with relatively slight undercutting of the film. The Pt (1000Å) film appeared to be suitable as a masking material for our anodization.

C. Anodization

A number of samples were anodized using different concentrations of HF and various current densities[2]. Ethanol was added to the solution to obtain a more hydrophobic etching surface and also served to minimize bubble formation. This enabled us to obtain smooth etching of the exposed circular patterns. To evaluate the porosity, the samples were oxidized, and the oxide removed. Once the oxide was etched, the depths of the formed trenches (the anodized material before oxidation) were measured. Knowledge of the depths, together with the overall geometry of the circular patterns, allowed us to calculate the volume of silicon that was converted into porous material. Mass measurements, before and after anodization, were taken. The difference in mass divided by the known volume of the porous material enabled us to calculate its porosity. In this way porousity data was obtained for a variety of anodization conditions. For example, 30 min in 20% HF with a current density of 20mA/cm^2 produced 37 microns of 65% porous material. The results, used for ploting and evaluation, were tabulated in Fig. 1.

Porosity was evaluated as a function of anodization conditions by varying: 1. The HF concentrations, 2. The anodization time, and 3. The current densities. The data indicates that porosity increases with decreasing HF concentration. Porosity was also found to increase with increasing current density (Fig. 2).

From these experiments it was determined that a 20%HF and 40% ethanol with a current density of 70mA would produce a porosity of about 70%. Such a porosity, after converting the porous material to oxide, was expected to result in complete closure of the anodized ring with minimal induced internal stress. It took up to 4 hours to anodize through the entire thickness of a 5 mil wafer sample. The end point was observed by noting the formation of pores at the back of these samples. The porosity was measured, as previously described above.

Section II: Conversion of Porous Si into SiO_2:

A series of samples, with circular patterns anodized through the wafer, were oxidized at various times and temperatures, and in different ambients. Most of the early samples warped and/or cracked during oxidation, as a result of the stress induced during the oxidation. These stresses result form two causes: The conversion of the porous silicon into SiO_2 results in a larger total volume than that of the original porous material. In fact, the original material represents only 45% of the final volume of SiO_2. In order to minimize this cause of internal compressive stress a somewhat higher initial porosity was chosen.

In addition, SiO_2 has a much lower thermal expansion coefficient than silicon (.5PPM/°C as compared to 2.6PPM/°C)[3]. As a

consequence when the oxidized material is cooled to room temperature, the SiO_2 is placed under a large compressive stress.

Factors such as: 1) Pore Morphology, 2) Porosity, and 3) Oxidation conditions probably influence the magnitude of total resulting compressive stress. It was determined that the asymmetrical-V-shaped geometry of the patterned porous region (see Fig 3) also contributed since the porosity varies with depth. It was, therefore, attempted to form a cone shaped geometry (Fig 3A) by anodizing from both sides of the wafer simultaneously. Patterns were fabricated using a "book mask" (The "book mask" allows the sample to be sandwiched between two aligned layers of Mylar masks during photolithography). The advantage of the later geometry is that its greater symmetry through the wafer thickness may compensate for and/or reduce the stress. At this time it was also decided to change the oxidized region from a circular area to a ring. This resulted in enclosing of an inner silicon region with a tubular like region of oxidized silicon. Moreover, by appropriate choice of geometry, a much smaller total volume of the wafer is made porous and subsequently converted to SiO_2. This not only lowers the total stress but also results in more unnoxidized silicon for greater strength and enhanced thermal conductivity.

In anodizing these samples, calculated time estimates were used to predict when the anodized regions from each side merged. By etching from both sides simultaneously, the total etchning time is cut in half not only reducing undercutting but also enhancing the durabilty of the masks. The first of the samples prepared using this "book masking" technique was oxidized at 700°C. This sample also broke, but the pieces were large enough to be evaluated. In addition, the breakage occurred during the cooling stage after the oxidation, and not during the oxidation itself, as in previous samples (i.e. V-shaped).

During the evaluation of the resulting pieces it was observed that the anodized regions were fully transparent to visible light. This indicates that the porous material was completely converted into SiO_2. Fig. 4 shows the ring pattern with the light source at the other end. This signified a major breakthrough since it was the first time anyone was able to convert silicon into oxide through the entire thickness of the wafer. The idea of forming oxide rings of isolation for the extended feedthroughs was demonstrated to be feasible.

Electrical isolation of the rings in the initial samples was tested at 30volts by contacting the field and the contact regions, within the oxide rings. The isolation current was found to be negligible ($<1\mu A$). The resitance of the feedthroughs was measured by contacting the contact regions from each side of the extended contacts cover-wafer. The resistance was found to be less than 1Ω.

Section III: Planarization of the Cover-Wafer

After the complete conversion of silicon into oxide was demonstrated, an effort to planarize and improve the morphology of the cover-wafers was undertaken. Structural symmetry, oxidation condition, and pore structure were targeted as the three areas crucial to the prevention of warpage and breakage.

1) Porosity

Although a detailed analysis of pore sizes and interpore spacing is essential to enable precise modeling of the entire process, it was found that overall porosity was the most significant variable.

In order to evaluate the pore size and the interpore spacing using Scanning Electron Microscopy (SEM), an attempt was made to analyze the cross section of the wafer. Various angles and magnifications were tried, but the pores were simply too small. this indicated that the pore sizes in P^+ material were less than 3000Å. Pores of such dimensions should be studied with Transmission Electron Microscopy (TEM).

Without knowing the exact pore sizes and interpore spacings, the porosity data, (based on previously mentioned density studies) was utilized to select the process conditions that had the best chance of resulting in hermetic oxide rings, while minimizing the level of built-in stress in the cover-wafer. As previously stated, during the oxidation process approximately 55% of the total volulme is supplied by oxygen while 45% of the total volume is supplied by the original silicon. However, porosity of about 70% was selected and utilized throughout the entire Phase I program in order to assure consistency for evaluating the effects of all the modifications to the process on the physical state of the cover-wafer, and to minimuze internal stresses. For process optimization, however, the internal structure must be better known.

2) Pin-Hole Free Masking Film

Pin-holes in the Pt mask were observed to lead to pit formation on the surface of the wafer during the anodization step[4]. These pits would later convert into oxide, just like all other anodized regions. The formation of these pits was completely non- symmetrical and therefore was probably a significant factor in inducing stress in the cover-wafer.

In order to reduce pinhole count in the Pt mask, a double layer of Pt was deposited on each side of the Si wafer. Specifically,

metal (Pt) layers of equal thickness were sequentially deposited with vacuum being broken in between the depositions. When a double-layer is used, the pinholes in each layer are not aligned, effectively resulting in a "pin-hole free" film. This film was used as a mask for anodization. Significant improvements were observed in the surface quality of the anodized layer (the pin-hole count was lower). During the oxidation step (porous Si converted into oxide), the samples with the Pt double layer exhibited reduced warpage compared to samples with the single Pt layer.

3) Modified Perparation/Oxidation Procedures

A new procedure was established whereby all porous material other than that in the complete tubular-like regions was removed prior to oxidation. These unwanted regions were areas around the ohmic contact (or contacts) to the wafer which also anodized from the back. These areas were dissimilar from the rest of the wafer and the resulting uneven oxidation acted as sources of stress. The new procedure also involved a slow thermal ramp-up during oxidation, in order to minimize thermal shock effects. The samples were laid flat, and elevated on a home made structure shown in Fig. 5 This procedure has resulted in samples being significantly more planar than before.

4) Modified "Book Masking" Technique

A modified "Book Mask" was designed to take into account the undercutting of silicon during the anodization process. This mask was assembled with more precision to enable a better overall alignment. The book mask is only used to make sure that the front-to-back registration is maintained but the resulting pattern in the photoresist is not sharp or well-defined. For that reason, additional exposures on each side were performed using a chrome-on-glass mask to produce enhanced images prior to

developing and etching.

5) Separate and Sequential Anodization

Separate and sequential anodization of each side of the wafer has resulted in a more symmetrical pore formation. In the earlier technique of simultaneous anodization of both sides, the contact (or contacts) were positioned on only one face of the wafer, leading to an uneven current density distribution, and resulted in asymmetrical anodization from front to back. Subsequent oxidation led to stress-induced warpage (attributed to the asymmetry of the pores).

The modified procedure, utilizing successive anodization with separate contacts for each side, resulted in a more symmetrical pore formation. The samples formed with this anodization procedure were then oxidized with the previously established procedure. This resulted in flat samples ready for bonding.

It was also noted the anodization rate was found not to be a linear function of time. The rate decreased as the anodization proceeded into the material. After three early tries, a complete anodization and conversion into oxide, extending through the entire thickness of the wafer, was achieved. The flatness of the wafer was preserved (Figs. 6A - 6D).

6) Process Modifications (Multi-Contact System and Wax Changes)

Upon a closer review of our previously developed symmetrical/sequential anodization process, further improvements were made. For example, anodization with a single contact was replaced with a multi-contact system to reduce variations in current density variations. This improved the uniformity of the anodization. In addition, wax, which was used as a mounting and

protection agent, was changed every 20 minutes, rather than having to withstand etching throughout the entire anodization. Rewaxing became necessary since, due to the non-uniformity anodization, certain portions of the wafer were breaking through, during final anodization step, while other portions were only nearing the end. Once the break-through occurred, wax was supposed to prevent the HF from attacking the back surface. However, traces of back surface degradation were observed. Rewaxing effectively solved this problem. Thus, increasing the number of contacts and re-waxing led to flatter samples and made the process more repeatable.

7) Simultaneous Anodization

A new approach to simultaneously etching the two sides while maintaing a complete symmetry was developed. This approach relies on being able to affix the sample in such a way so as to provide an electrical contact to both sides at once. The samples were mounted and contacted as shown in Fig. 7. After their mounting the samples were anodized (both sides being anodized simultaneously) and oxidized. This procedure produced fairly planar samples. More work should be done in this area to compare and contrast the sequential anodization and the simultaneous processes. It is clear that anything that insures a more uniform current density during the etching will insure a more uniform porosity and result in more stress-free wafers. The one clear potential advantage of the simutaneous process is the time saving during the anodization.

8) Alternative Processes

Alternative processes for fabricating the desired cover-wafer with extended feedtroughs were also investigated. An approach was based on the idea that the amount of warpage in the final

encapsulation layer/wafer, containing the feedthroughs, could be completely eliminated if this layer/wafer was attached to a relatively thick support wafer prior to the oxidation step. To achieve this, a 5.5-mil P^+ was fusion bonded to a 10-mil thick N-type support wafer. However, the anodization and oxidation processes performed on the P^+ wafer resulted in significant warpage of the joined structure, with the anodized face being in tension. It was presumed that the anodization proceeded much further into the N-Type material than expected, since the indents (imprints) of anodized patterns actually became visible on the back side of the N-type wafer. In order to demonstrate the feasibility of this alternative process, without spending a great deal of time on establishing an appropriate anodization procedure, another process was carried out. An N-type wafer deeply diffused with a p^+ dopant was fusion bonded to another N-type support wafer. After the bonding, a conductivity selective etch (Hydrazine) was utilized to remove all the N-type silicon from the first wafer, thereby leaving the p^+ diffused layer on the surface of the support wafer (Fig.s 8A - 8B)[5]. The thickness of the p^+ layer was measured to be around .4 mil. The appropriate anodization parameters were selected to anodize the p^+ layer without proceeding much further after that. The criticality of the error, associated with stoping at exactly the correct time, was drastically minimized from the previous experiment since relatively short times are needed to anodize .4 mil of silicon. The first attempt to anodize the diffused layer with previously chosen parameters resulted in the layer being completely etched (100% porosity). This result is consistent with the previously known relation of porosity dependency on doping levels[6]. The diffused sample had sheet resistance of .6Ω/□ (≈.0006Ω-cm resistivity). Since the resistivity of this sample was significantly lower than that of the previously utilized wafers, higher porosities, for the same anodization, conditions were

expected. Reduction of the current density to 40mA/cm^2 still resulted in silicon being removed. However, current densities of 10mA/cm^2 and 20mA/cm resulted in porous silicon films with reduced porosities. After performing the anodization and oxidation steps the joint structure was completely flat. The contact to contact isolation, at 50 Volts, was confirmed. Profilometric measurement indicated no change in surface morphology.

Section IV: Cross Sectional Analysis and Surface Morphology

A) Evaluation of the Surface Profiles of Anodized Regions Post-Oxidation:

The surface profiles of the oxidized cover-wafer were evaluated. SEM photographs (fig. 9) showed an elevation of the undercut regions above both the anodized and non-anodized regions. Surface profilometry (see fig. 10) shows that the undercut regions are elevated above the surface of the anodized regions by roughly 1 micron, while the anodized ring-areas are elevated above the non-anodized silicon by around 5 microns. This data indicated that the elevated oxide surface (6 microns) must be etched down prior to bonding. A very detailed study of anodization conditions vs oxide elevation is required.

B) Cross Sectional Evaluation of Anodized Regions after the Oxidation:

A silicon through-wafer interconnect is shown in figures 11A & 11B. This interconnect was obtained by etching a cover-wafer (post-oxidation) in HF to remove the SiO_2. Figures 11A & 11B depict a dependence of silicon-interconnect structure/morphology

on crystallographic direction. In one direction a nearly cylindrical interconnect is formed, while in the other direction the interconnect exhibits a more conical structure. These differences in shape are likely associated with the dependence of anodization rate on crystallographic direction. This effect is also observed in the mask undercutting (see fig. 10), whereby a masked circular area evolved on to an elliptical shape during. anodization. The crystallographic dependency of anodization also needs to be studied further.

Figure 4 confirms that the anodization procedure resulted in an isolated silicon pole formed through the entire thickness of the wafer. The exact shape of the poles was also confirmed to resemble back to back pyramids attached to one another.

C) Evaluation of the surface smoothness of the completed cover-wafer.

After we first started to work on improving the flatness of the cover-wafers, the stress lines, visible only after oxidation, and not after anodization, were observed (Fig. 12). The quantity of these lines has been reduced drastically during successive modifications to the cover-wafer fabrication process. It is presumed that the reason these lines become visible after oxidation is atributed to expansion of oxide and the state of stress that the wafer is put in. Surface deformation, roughness, is a common relief mechanism for stress outside of wafer warpage.

Section V: Fabrication Methods for Sensors Compatible with Cover Wafers.

The diffused piezorestive device wafers described in previous

reports were fabricated and tested. In these wafers, the contacts and the sealing areas around the device are elevated with respect to the diffused pattern. In this way, the cover wafer can be sealed to the raised areas not only making an ohmic contact but also hermetically sealing the device (fig. 13).

The individual sensors were evaluated prior to sealing and were found to be consistent with standard devices. These sensors are now ready to be bonded to cover wafers and will be so used in the next stage of the research. It is anticipated that both gold - silicon, and aluminum - silicon eutectic bonding will be used to affect seals between the cover wafer and the sensor wafer. A dielectrically - isolated high temperature sensor was designed to be compatible with the cover-wafer sealing process[7]. In this sensor configuration, the grid, contact areas and the sensor network are all fusion bonded to a carrier wafer which contains a dielectric isolating layer [8] copy enclosed in appendix. In order to seal such a wafer to the cover wafer, one must provide a depression in the cover wafer in the active area of the sensor to insure that the sensor network is not sealed to the cover wafer. The drawings for the new sensor wafer and the new cover wafer are shown in figure 14. Future work will concentrate on fabricating both the new sensor as well as the re-designed cover wafer.

Section VI: Hermetic and Dielectric Isolation of Cover - Wafer/Process

A) The hermetic isolation of the cover-wafers was established with the aid of a helium leak detector. The cover-wafers with oxidized rings of isolation were placed on leak detector (with the aid of o-rings) as shown in figure 15. No leakage was observed on a 3×10^{-7} cc/sec scale signifying hermeticity of the cover-wafer.

B) The electrical isolation of the Si feed-throughs was evaluated. The oxide breakdown occurred at 550 volts. Up to 550 volts a complete isolation of the feed-throughs to the field and/or to other feed-throughs was observed.

C) The hermeticity of the process was evaluated by first attaching a silicon sample with a hole to a completed sensor chip and then evaluating the hermeticity of the seal with the aid of a leak detector (fig. 16). The joining of the sensor die to the silicon sample was performed utilizing the aluminum metal, used for contacting the piezoresistive pattern, and executed in a rapid thermal annealer at temperatures in excess of the melting point of aluminum. The process was found to be completely hermetic on a 3×10^{-6} cc/sec scale of the helium leak detector. Since the process of establishing dielectrically isolated contacts through the silicon wafers was previously developed, the ability of attaching silicon to customized sensor chips demonstrates the feasibility of hermetically encapsulating sensor devices. The type of sensor implemented, the type of joining technique, and the evaluation of contact quality should be further studied in order to establish a working prototype of an encapsulated pressure sensor.

Conclusion

During the course of this work novel processing techniques were developed for encapsulating pressure sensors with hermetically sealed, dielectrically isolated extended contacts through the entire thickness of the wafer. Conversion of single crystal

silicon into porous silicon and subsequent conversion of porous silicon into silicon dioxide has been carefully studied and processes for fabricating cover-wafers with extended feed-through were developed. The hermeticity and the dielectric isolation of these wafers were demonstrated. The fabrication process was modified to optimize the planarity and surface morphology of the cover wafer. These improvements resulted of smooth cover wafers customized for sealing to device wafers. Sensor wafers, both diffused and dielectrically isolated, suitable for sealing to cover wafers were designed. The diffused wafers were fabricated and evaluated, and were found to be adequate for processing to cover wafers. Dielectrically isolated structures suitable for further processing will be fabricated in the next phase of the work.

More detailed characterization and process development has the potential to produce a new generation of environmentally protected microsensors and other types of devices, with the encapsulation performed in the wafer stage. This has far-reaching implications not only in the field of microsensors but also in the entire area of solid state device technology.

REFERENCES

1. Handbook of Thin Film Technology edited by Lean I. Maissel and Reinhard Glang, McGraw-Hill Book Co., NY 1970. Pages 6-28 to 6-32.

2. R.L. Smith and S.D. Collins: J. Appl. Phys. 71, R1 (1992).

3. Silicon Processing for the VLSI Era Volume 1 - Process Technology. S. Wolf and R.N.Tabber; Latice Press, CA 1986.

4. Handbook of Thin Film Technology edited by Lean I. Maissel and Reinhard Glang, McGraw-Hill Book Co., NY 1970. Pages 7-46 to 7-48.

5. S.S. Wang, V.M. McNeil and M.A. Schmidt, ibid 7 p. 819.

6. V. Lehmann and V. Gosele, Applied Physics Lett. 58,856 1991.

7. U.S. Patent # 4,672,354 issued to A.D. Kurtz, T.A. Nunn, and R.A. Weber of Kulite Semiconductor Products, Inc. June 9, 1987.

8. U.S. Patent #5,286,671 issued to A.D. Kurtz and A.A. Ned of Kulite Semiconductor Products, Inc., Feb. 15, 1994 (copy is enclosed in the Appendix I).

Figure 1

Porosity Data

Sample #	Electrolyte Conc.	Current Density(mA/cm^2)	Anodization Time (min)	Depth (μ m)	Weight Change (mg)	Porosity (%)
Sip3-1	10%HF	20	60	45	10.31	75
Sip26-1	20%HF_20%Ethanol	5.6	240	120	.5234	30
Sip4-1	"	20	60	53	8.59	55
Sip10-1	"	20	150	137.5	0.865	50
Sip5-1	"	30	30	37	7.4	65
Sip8-1	25%HF_20%Ethanol	20	15	22	0.6766	40
Sip7-1	"	30	15	28	0.7	43
Sip9-1	"	40	15	30	0.692	55
Sip11-1	10%HF_10%Ethanol	22.6	180	80	1.0199	72
Sip12-1	"	20	180	75	1.0519	70
Sip48-1	20%HF_40%Ethanol	70	60	140	4.72177	75
Sip49-1	"	60	60	140	4.6646	65
Sip50-1	"	70	110	140		70

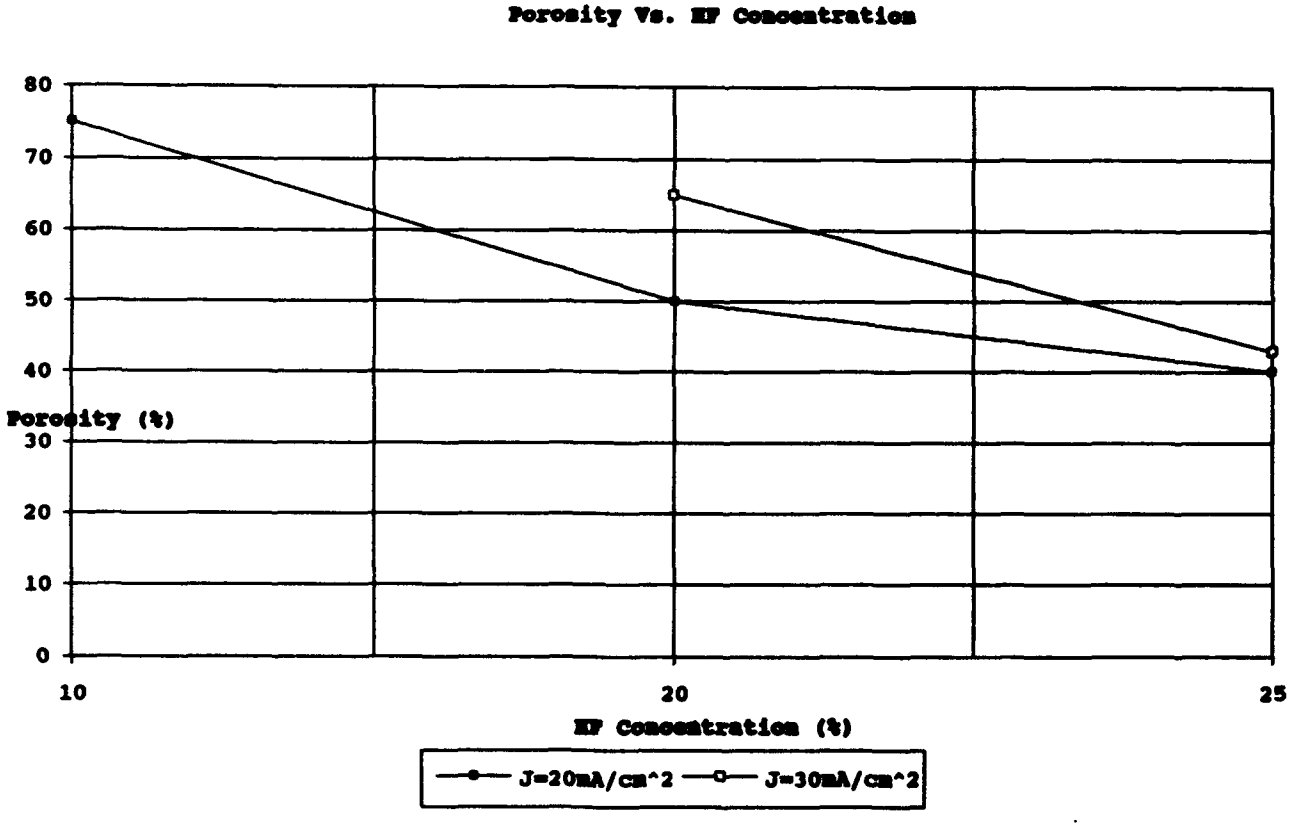


Fig. 2A

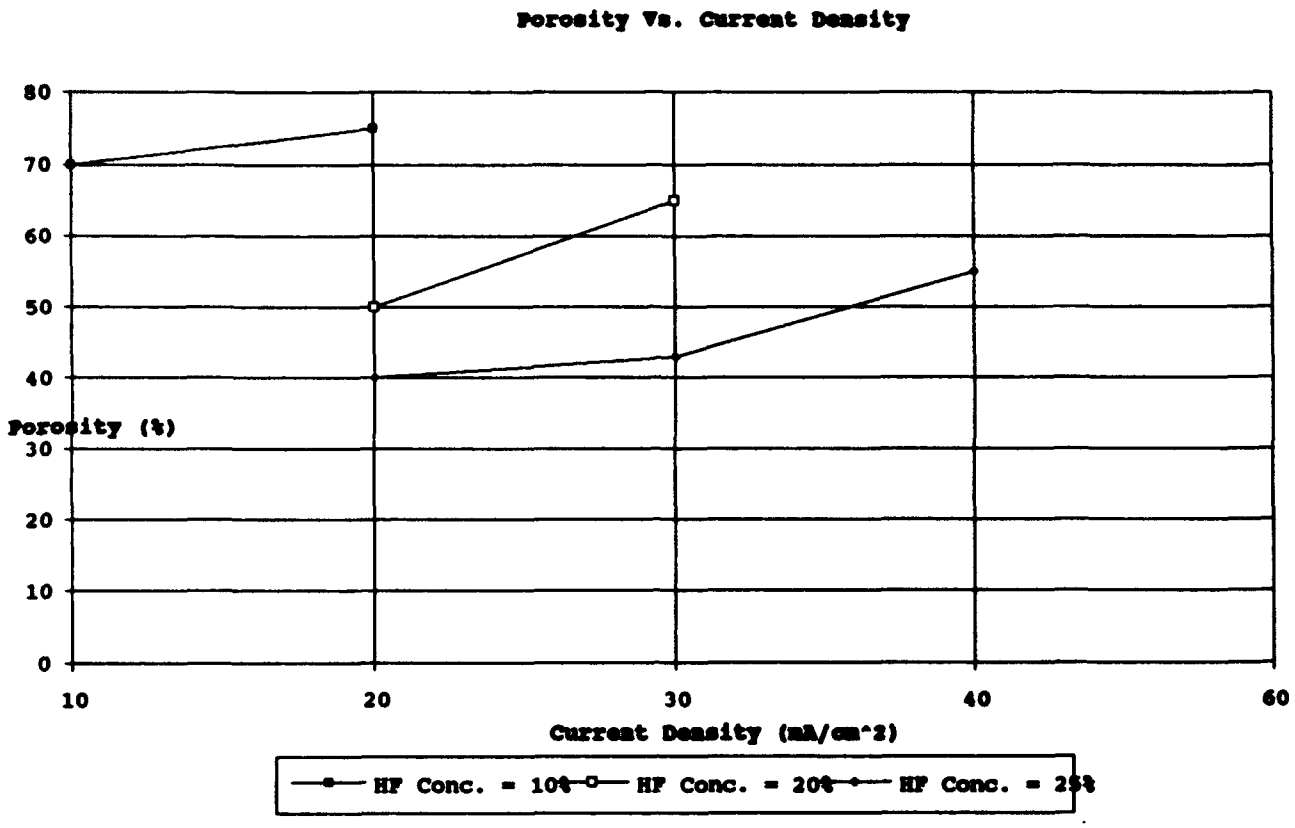


Fig. 2B

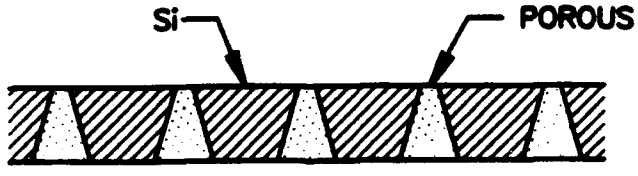


Fig. 3

V-SHAPED GEOMETRY

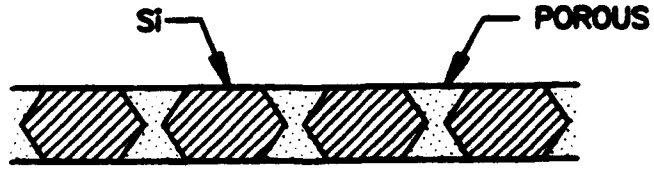


Fig. 3a

BACK TO BACK CONE-SHAPED GEOMETRY

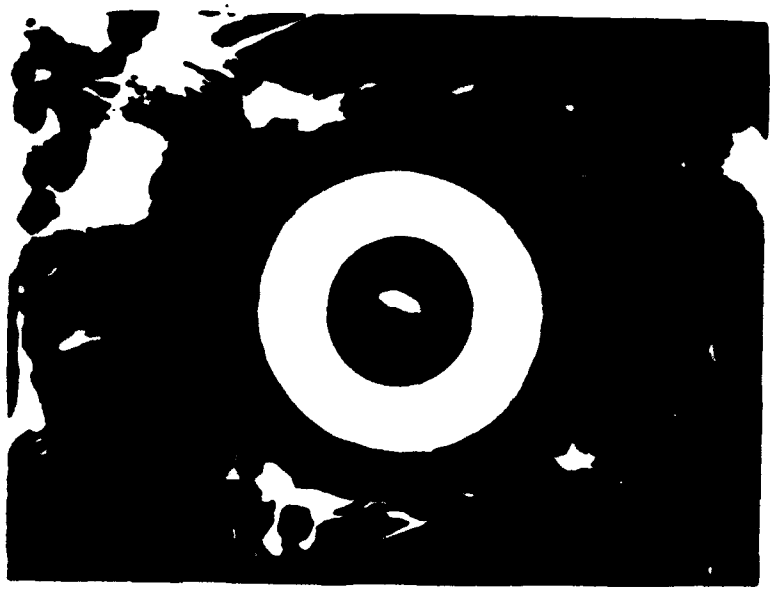


Fig. 4
Magnified Top View of an Oxidized Feed Through Light Source Coming From the Other Side.

Fig. 4B
Silicon Dioxide's Uniform Transparancies.

Fig. 5

Cover-Wafer Holder
for Oxidation Step

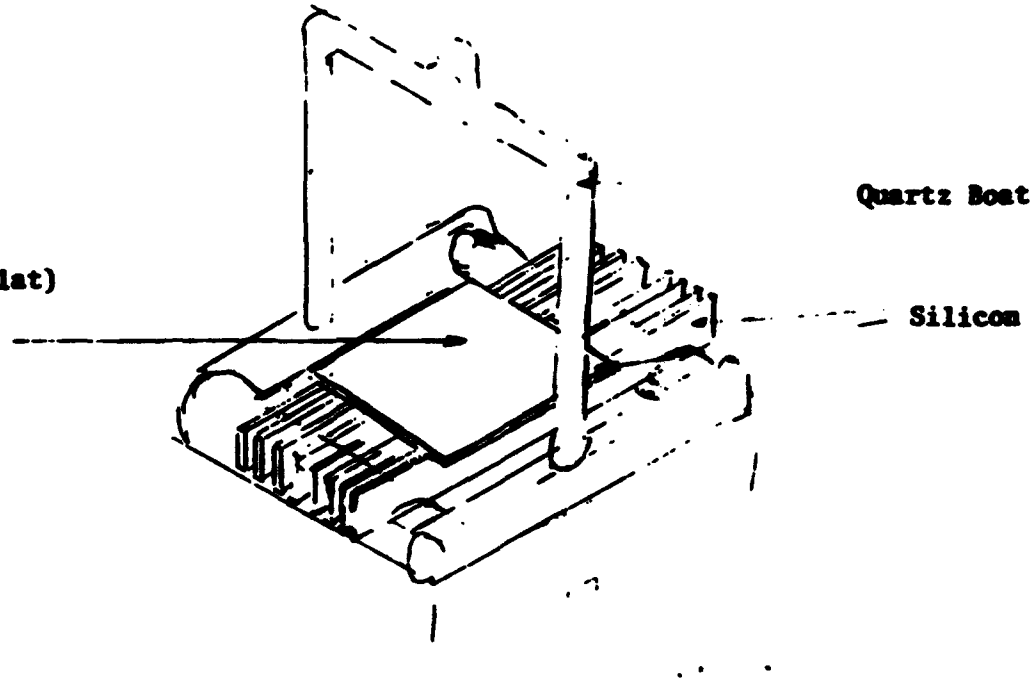


Fig. 6A
Side-view
cover-wafer

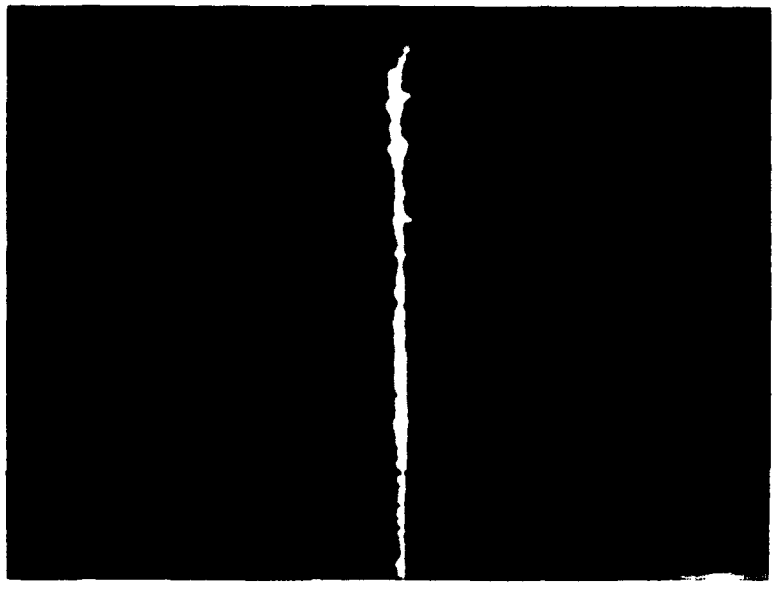


Fig. 6B
Side-View
cover-wafer

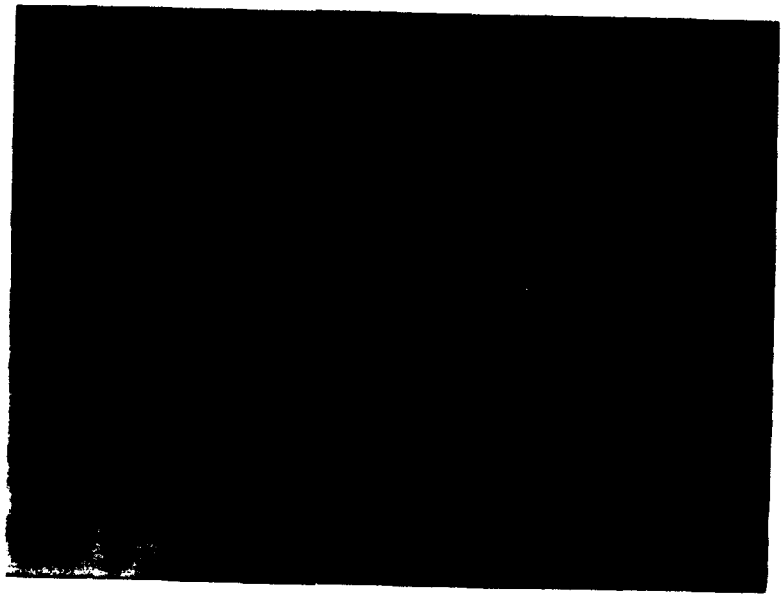


Fig. 6C
Top-view
cover-wafer

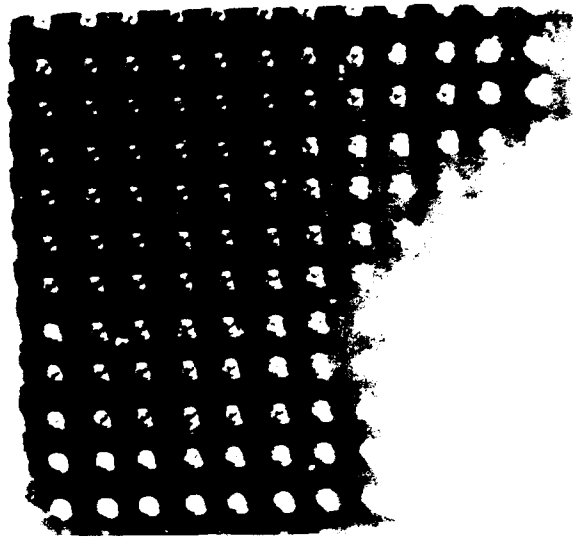


Fig. 6D
Top-View
Magnified
cover-wafer

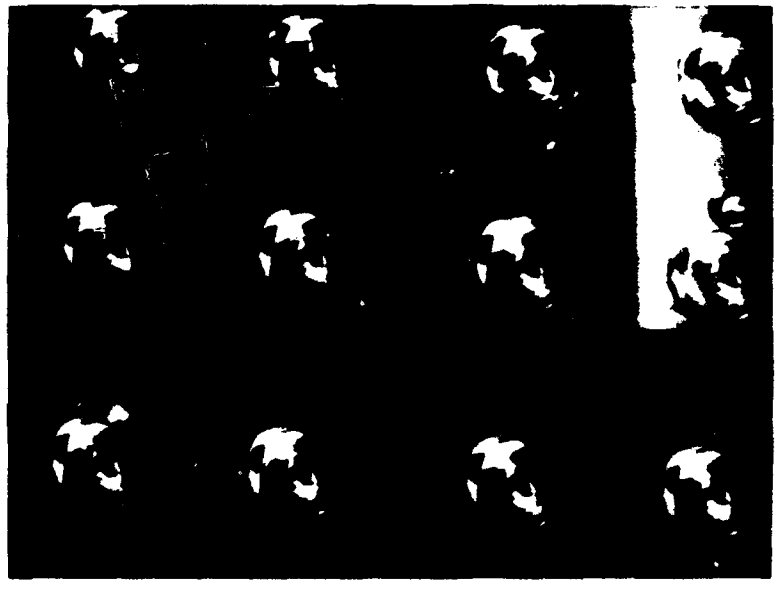
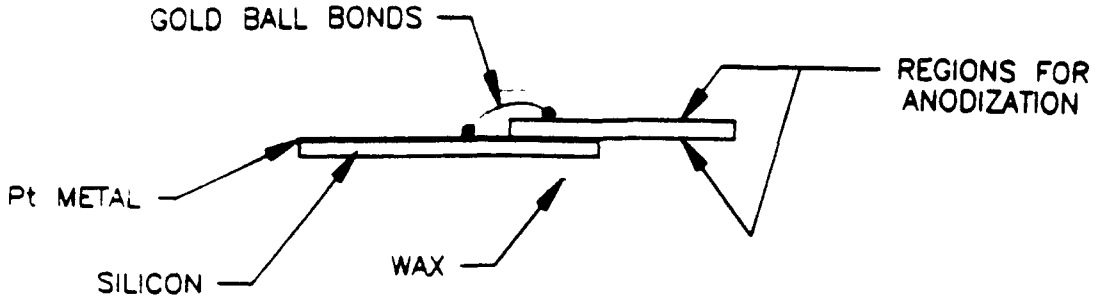
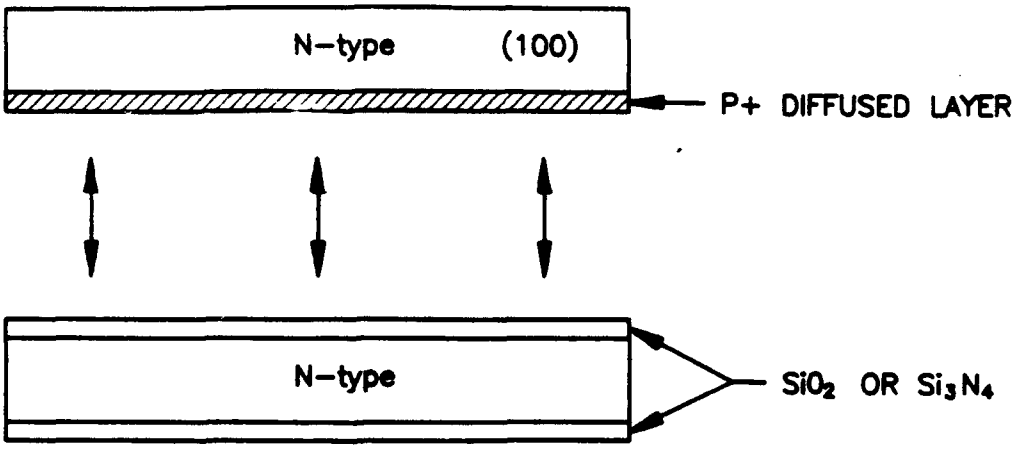


Fig. 7



ALTERNATIVE PROCESS

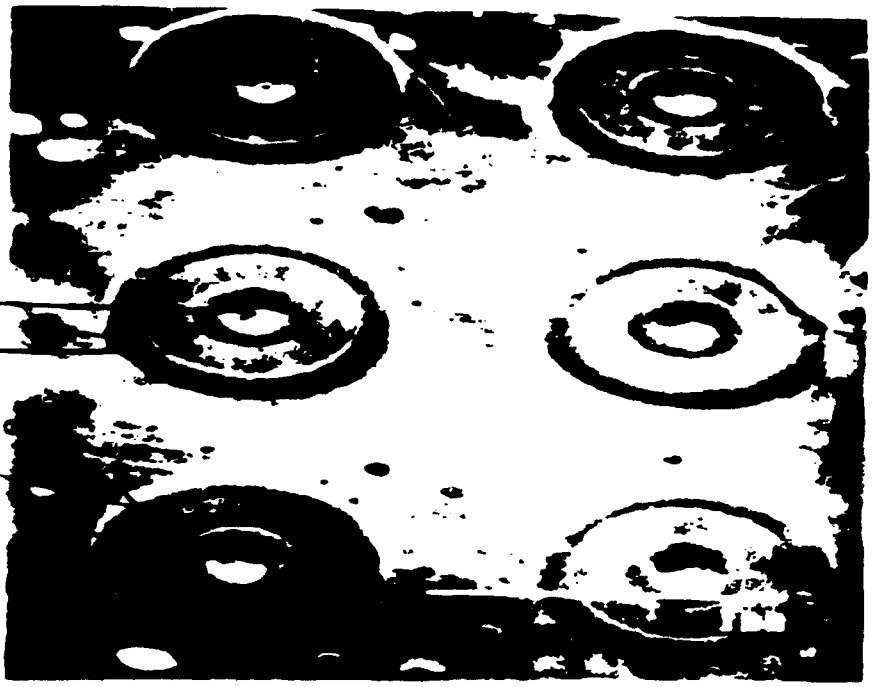
Fig. 8a



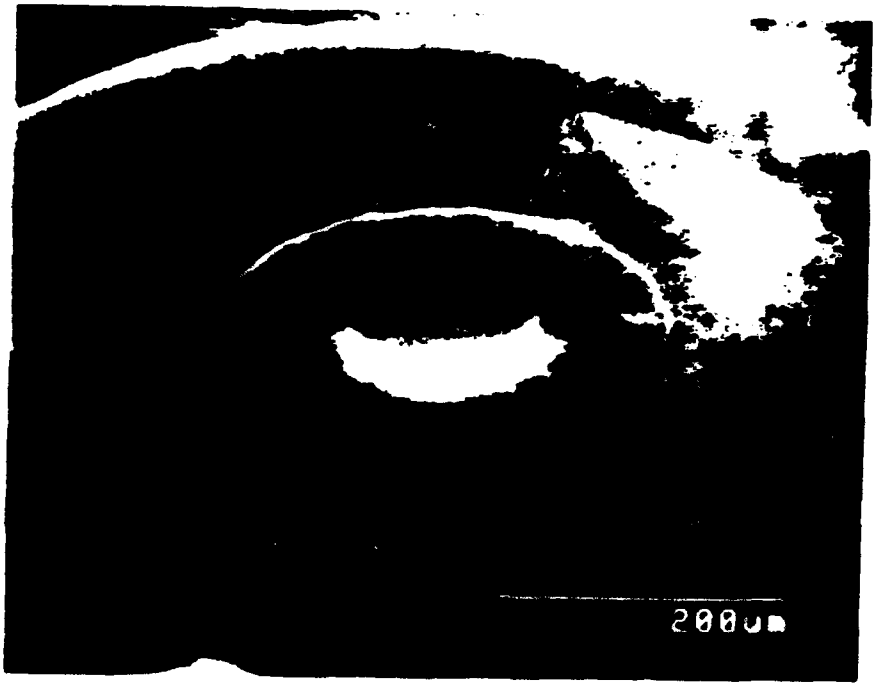
AFTER SELECTIVELY ETCHING THE N-type MATERIAL

Fig. 8b

a) Six Patterns



b) Magnified view of one pattern.



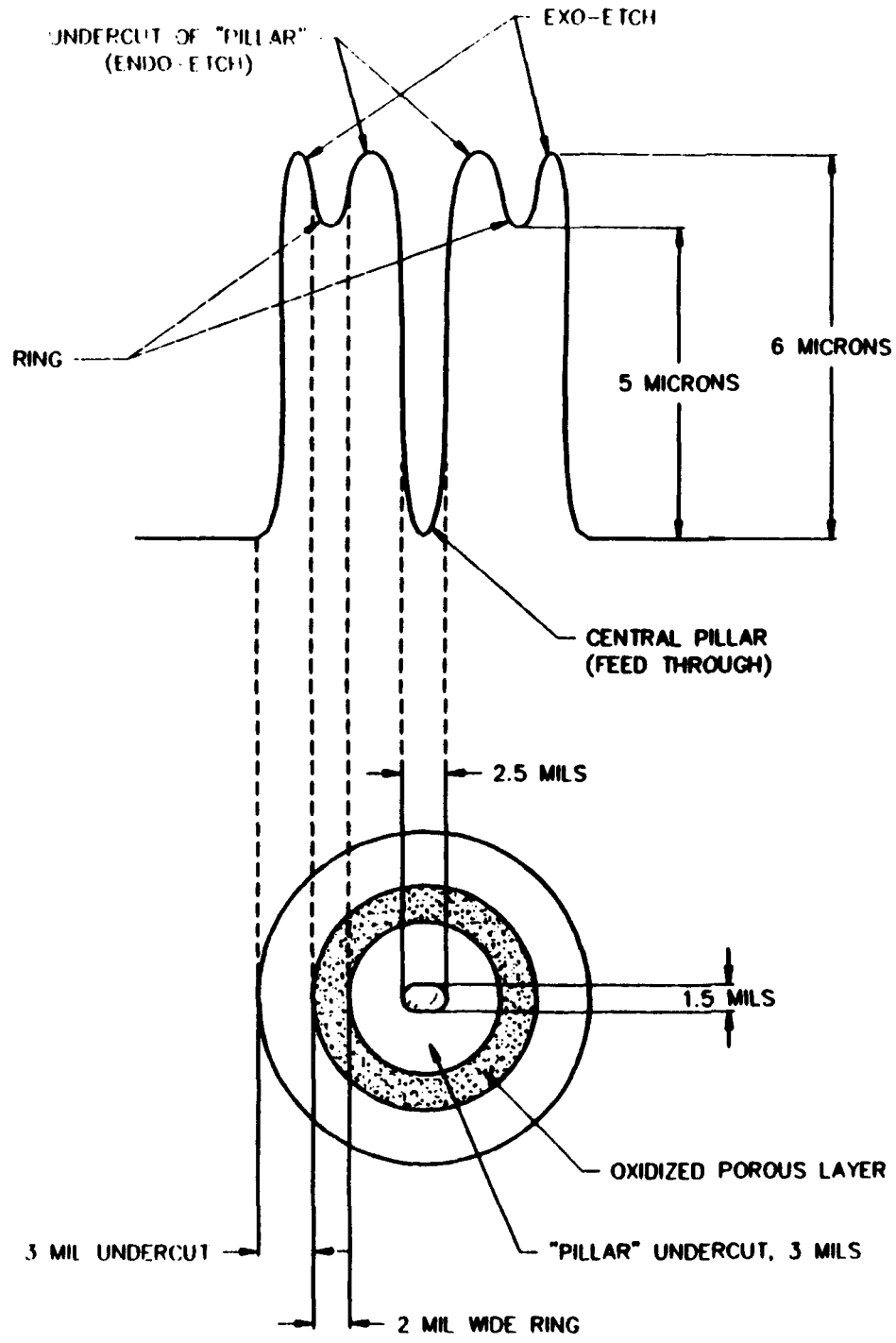


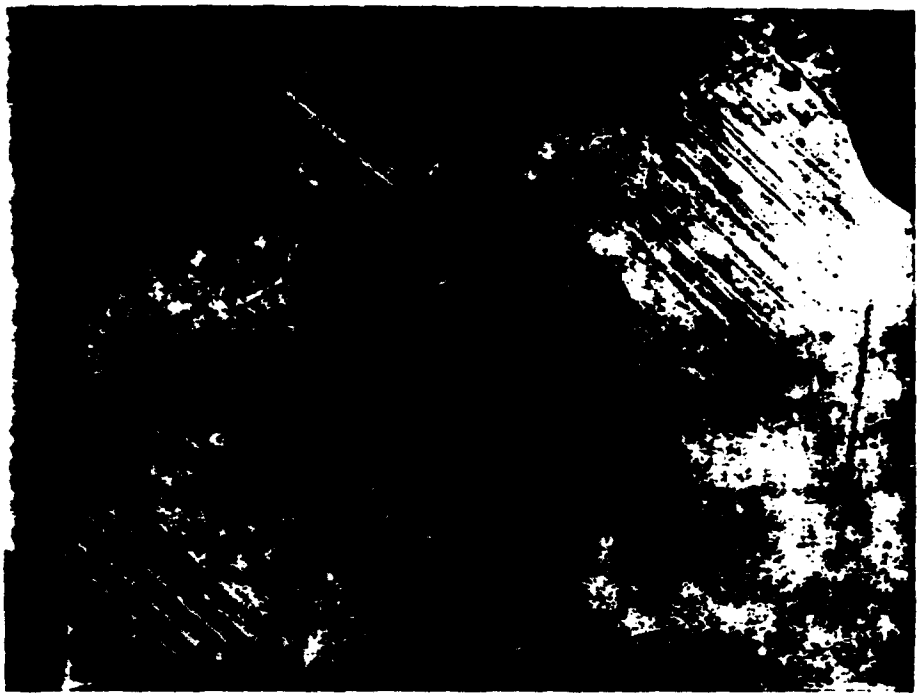
Figure 10: Surface Profilometry and Appearance

Fig. 1 1 Individual Interconnects (Middle Poles) separated from the rest of the donut patterns.

a) Silicon Feedthrough (Middle Pole). One view angle.

b) Silicon Feedthrough (Middle Pole). Second view angle.

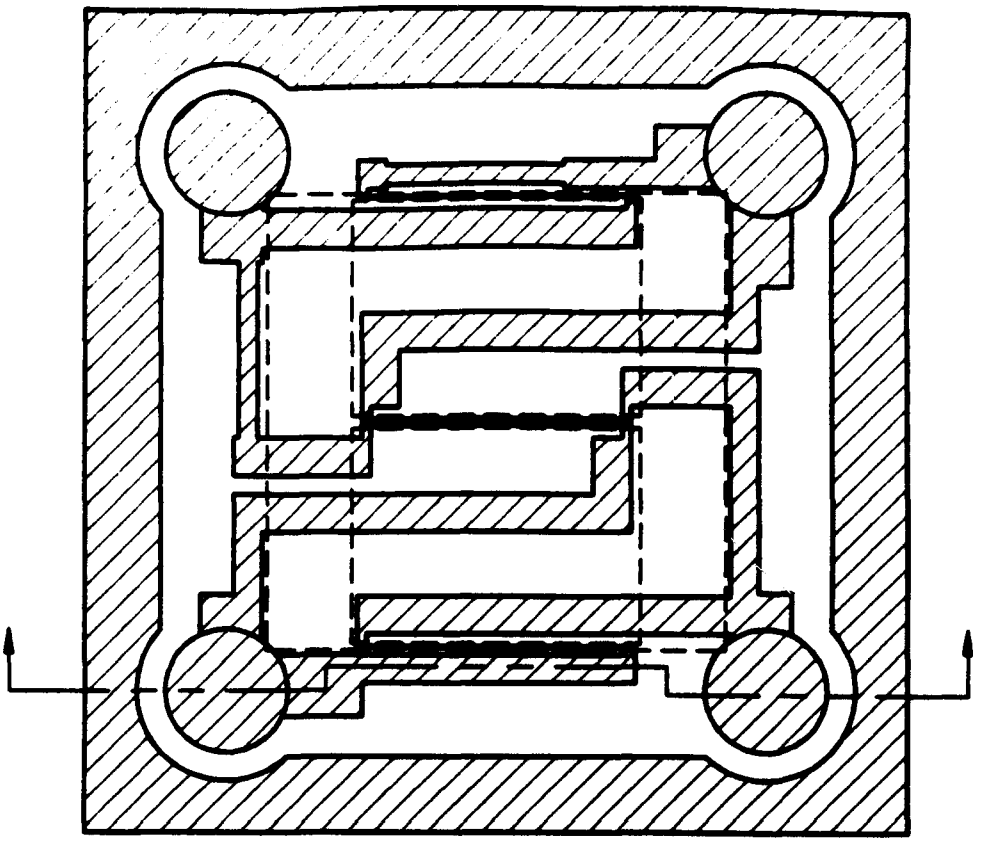
Fig. 12
Stress Lines
Magnified



SENSOR DESIGN COMPATIBLE WITH COVER-WAFER ENCAPSULATION

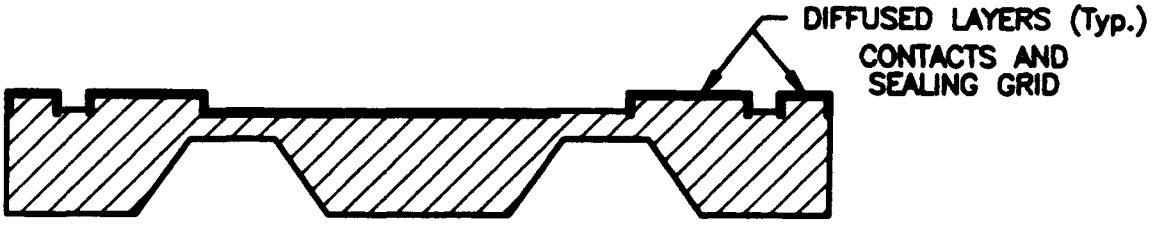
Figs. 13a & 13b

FIG. 13a
(Top View)



DIFFUSED PATTERN LAYOUT

FIG. 13b
(Side View)



RAISED CONTACTS

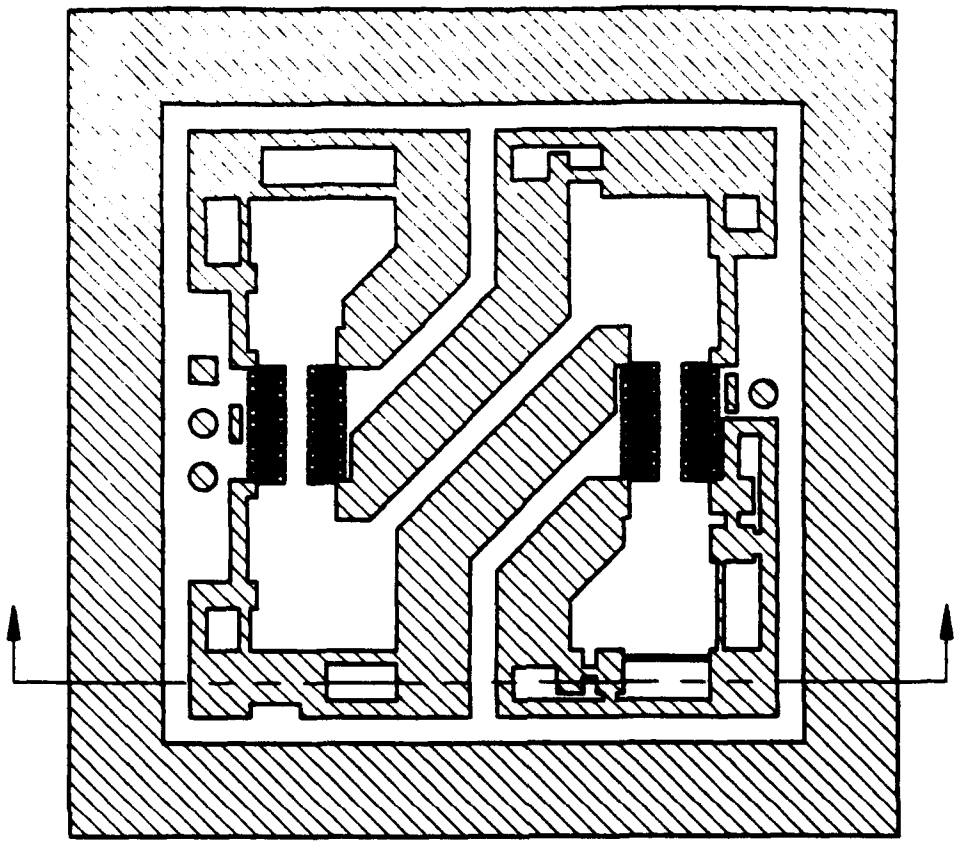


Fig. 14a

SENSOR WAFER
(TOP VIEW)

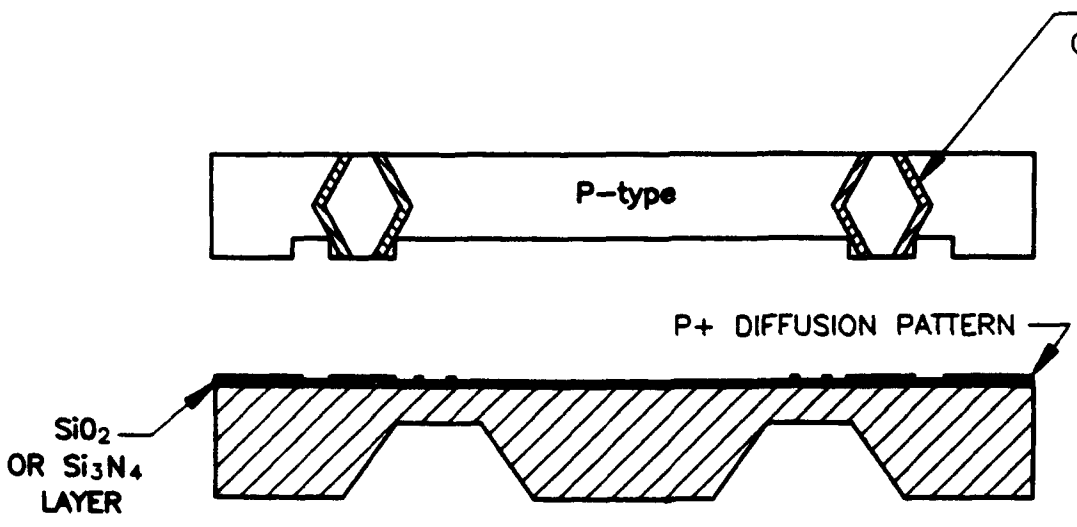


Fig. 14b

SENSOR & COVER
WAFER SET
(SIDE VIEW)

ISOLATED "EPI" DIFFUSED LAYER

COVER-WAFER HERMETICITY EVALUATION UTILIZING THE LEAK DETECTOR TEST

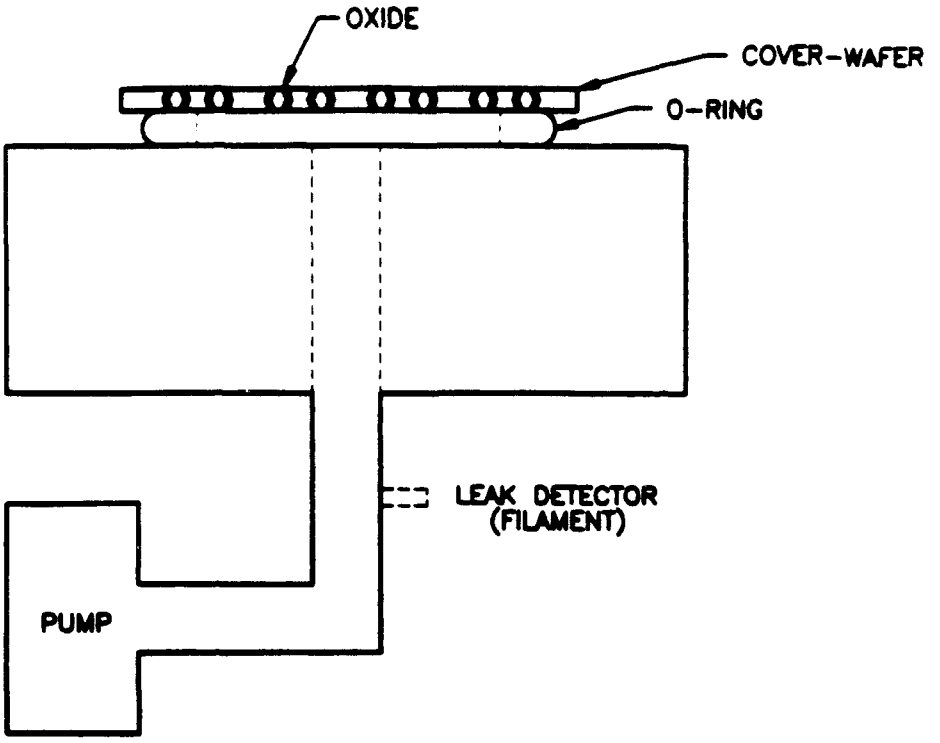


Fig. 15

PROCESS HERMETICITY EVALUATION UTILIZING THE LEAK DETECTOR TEST

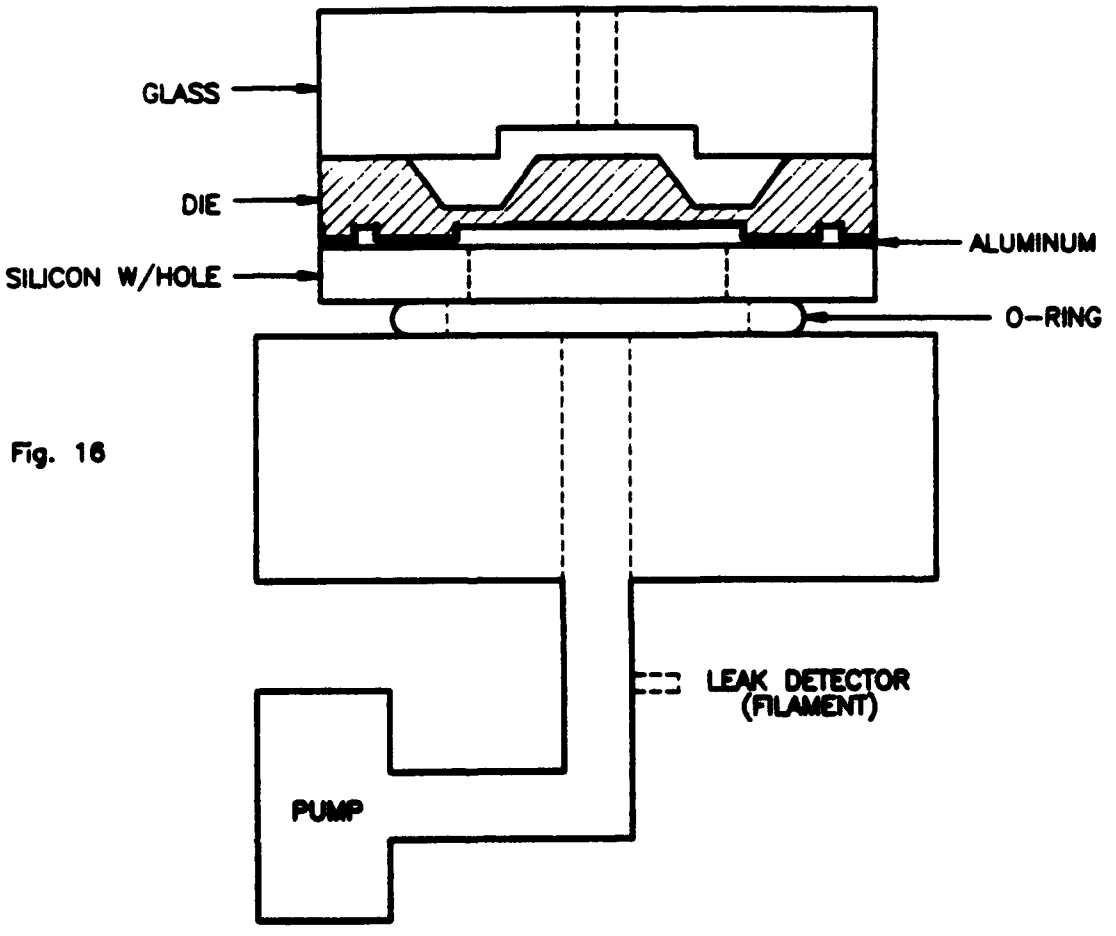


Fig. 16

US005286671A

United States Patent [19]

Kurtz et al.

[11] Patent Number: 5,286,671

[45] Date of Patent: Feb. 15, 1994

[54] **FUSION BONDING TECHNIQUE FOR USE IN FABRICATING SEMICONDUCTOR DEVICES**

[75] Inventors: Anthony D. Kurtz, Teaneck; Alexander A. Ned, Bloomingdale, both of N.J.

[73] Assignee: Kulite Semiconductor Products, Inc., Leonia, N.J.

[21] Appl. No.: 58,480

[22] Filed: May 7, 1993

[51] Int. Cl.[5] H01L 21/306

[52] U.S. Cl. 437/64; 437/901; 148/DIG. 12

[58] Field of Search ..... 437/62, 63, 64, 65, 437/901, 925, 966, 974; 148/DIG. 12, DIG. 135, DIG. 150

[56] References Cited

U.S. PATENT DOCUMENTS

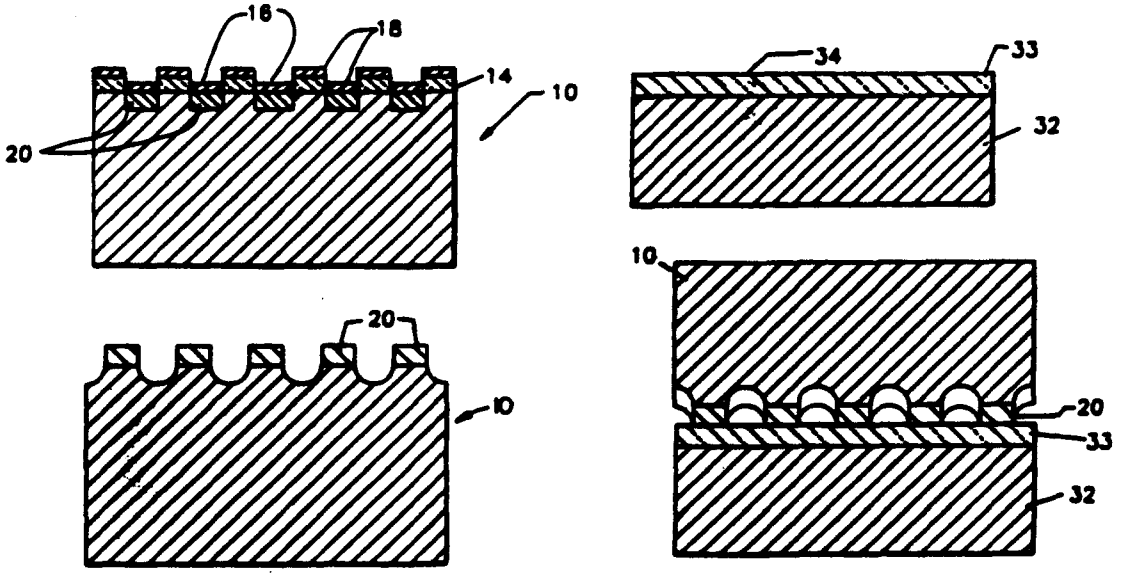
3,924,322	12/1975	Kurtz et al.	437/901
4,498,229	2/1985	Wilner	437/901
4,638,552	1/1987	Shimbo et al.	148/DIG. 12
4,672,754	6/1987	Kurtz et al.	437/901
5,238,865	8/1993	Eguchi	148/DIG. 12

Primary Examiner—Brian E. Hearn
Assistant Examiner—Chandra Chaudhari
Attorney, Agent, or Firm—Arthur L. Plevy

[57] **ABSTRACT**

A method of bonding a first silicon wafer to a second silicon wafer comprises the steps of diffusing a high conductivity pattern into a surface of a first semiconductor wafer, etching a portion of the surface to raise at least a portion of the pattern, providing a second semiconductor wafer having an insulating layer of a silicon compound disposed thereon, contacting the surface of the pattern to the insulating layer, and bonding the first and second semiconductor wafers at an elevated temperature.

16 Claims, 4 Drawing Sheets



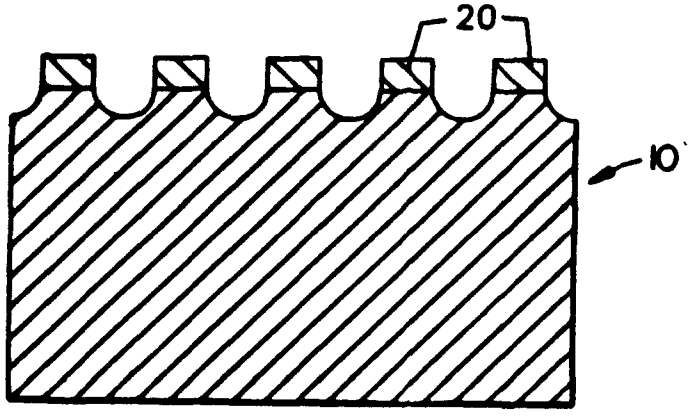


FIG. 5

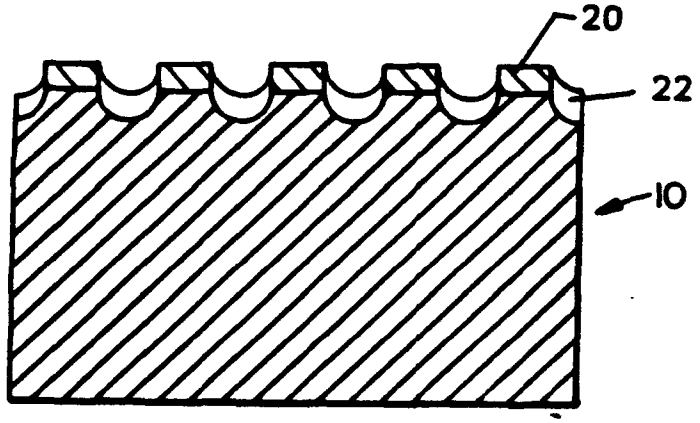


FIG. 6

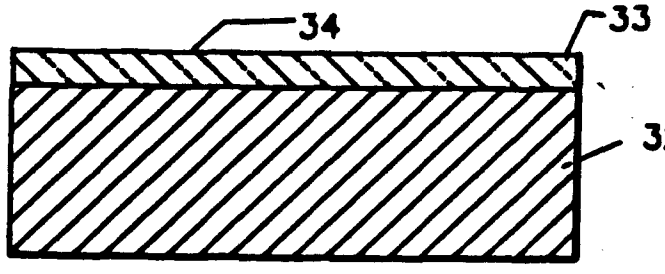


FIG. 7

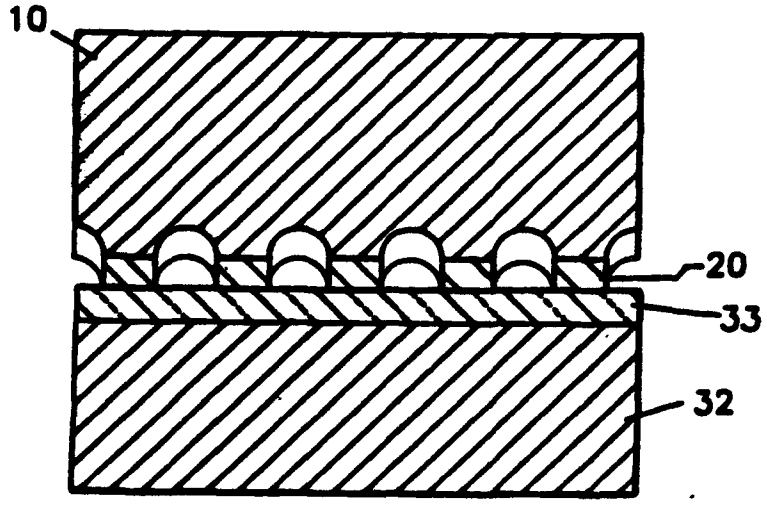


FIG.8

THIS
PAGE
IS
MISSING
IN
ORIGINAL
DOCUMENT

3 of 4

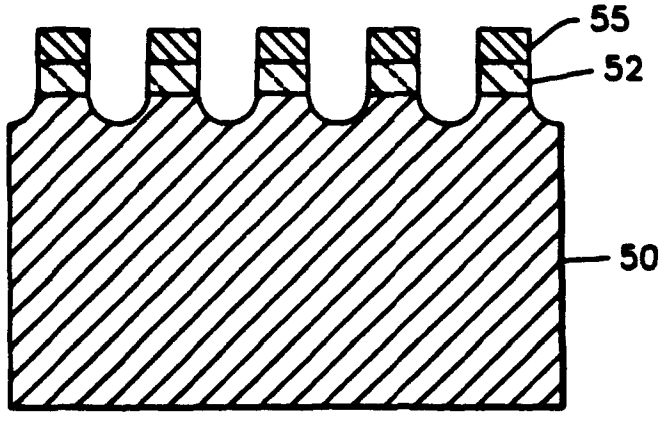


FIG. 13

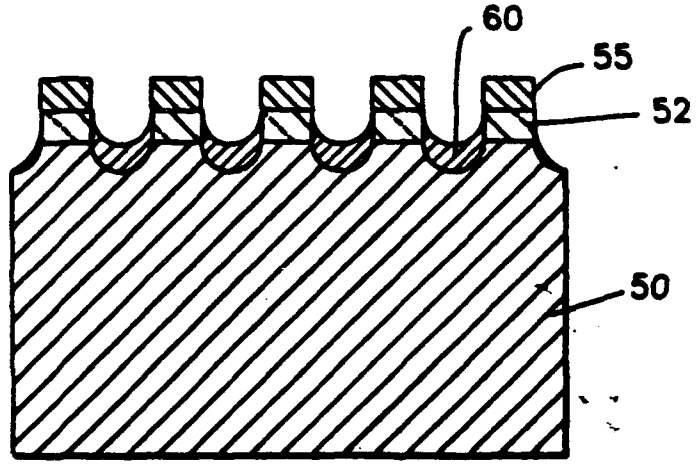


FIG. 14

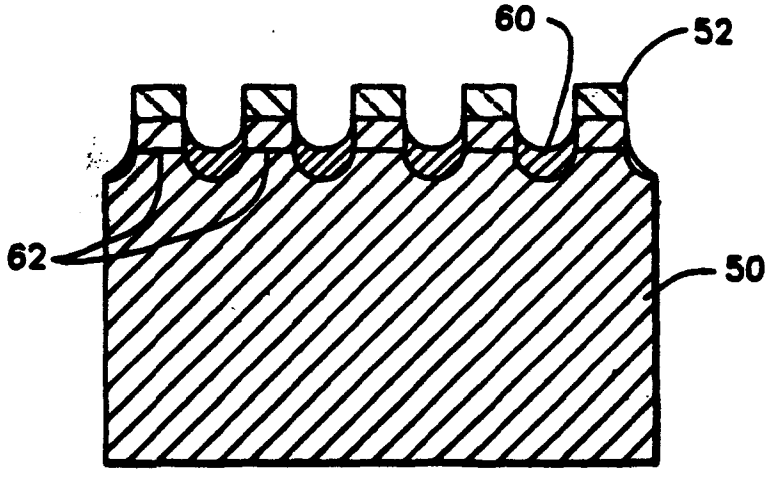


FIG. 15

FIG. 8 is a cross sectional view showing a device wafer which has been fusion bonded to a handle wafer in accordance with the inventive method.

FIGS. 9–15 are cross sectional views depicting a process for fabricating a device wafer for fusion bonding in accordance with another embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Before proceeding with the detailed description, it should be understood that although the specification will make reference to a piezoresistive transducer in which piezoresistive elements are incorporated in a bridge configuration on a substrate, the inventive technique for fusion bonding two silicon wafers described herein is not to be limited to transducer devices and may, in fact, be utilized to fabricate SOI wafers for a wide variety of electronic devices, including power devices and sensors generally.

With reference now to FIG. 1, there is shown a cross sectional view of a treated device wafer 10. The original device wafer 10 may be fabricated from a semiconductor material, such as N-type silicon, and is preferably a single crystal structure. The wafer may be circular or rectangular in the top plan view. Essentially, such wafers are commercially available and are well known in the art. According to the first method to be described, the surface 12 of wafer 10 is polished or lapped to a smooth finish. The polishing step is such as to almost produce an optical flat. The wafer 10 is then treated so that an oxide layer 14, which may be 5000 angstroms thick, is grown on a surface thereof, as shown in FIG. 2. The growth of oxide layers on silicon substrates is well known in the art and is described in many references. A typical technique for providing an oxide layer on a silicon substrate is implemented by heating the wafer 10 to a temperature between 1000°–1300° C. and passing oxygen over the surface of the substrate.

With reference now to FIG. 3, it can be seen that the desired device patterns 20 are now defined in the oxide layer wafer 14. This is accomplished by the use of photolithography, a well known technique in the semiconductor art. Briefly, the photolithographic technique involves the preferential removal of the oxide layer 14 by spreading a uniform photosensitive film over the oxide, masking portions of the film and exposing the assembly to ultraviolet radiation. The exposed portion of the film becomes insoluble, whereas the masked portion is soluble in a developing film. The oxide in those areas where the film has been removed can now be removed by etching in hydrofluoric acid, thus providing openings 16 in the oxide layer corresponding to the desired patterns.

As shown in FIG. 4, the substrate is again oxidized to form an additional oxide layer 18, which may be on the order of 1000 angstroms, over oxide layer 14 and the etched openings 16. It is well known that one may diffuse various impurities into a silicon wafer through an SiO_x layer. Thermal oxides are very smooth and, unlike most of the deposited films, their microroughness is not detectable by stylus profilometry or Normarsky optical microscopy. The desired device patterns, which for purposes of illustration are piezoresistive bridge patterns 20, are predefined by degenerately prediffusing a P-type impurity such as boron through the openings 16 and the thin oxide layer 18 into the N-type device wafer 10. This may be accomplished by diffusing B_2H_6 into the device wafer 10 for approximately 30–35 minutes at 1150° C., which results in a sheet resistivity of about 5–10 ohms per square.

As is well known, semiconductor transducers typically employs one or more piezoresistive elements which are mounted or diffused in a bridge pattern of resistors on a thin diaphragm member. The diaphragm member, which may be fabricated from silicon, flexes upon application of force thereto and thereby causes fiber stresses on the top surface. These stresses elongate or shorten the piezoresistors and cause them to vary their resistance according to the deflection of the diaphragm. Reference may be had to U.S. Pat. No. 4,498,229 entitled PIEZORESISTIVE TRANSDUCER, issued on Feb. 12, 1985 to Leslie B. Wilner and to U.S. Pat. No. 4,672,354 entitled FABRICATION OF DIELECTRICALLY ISOLATED FINE LINE SEMICONDUCTOR TRANSDUCERS AND APPARATUS, issued on Jun. 9, 1987 to Anthony D. Kurtz et al., assigned to the assignee herein, as illustrative examples of piezoresistive transducer construction. It is, of course, understood, that many pattern configurations can be accommodated on a silicon wafer 30, strictly dependent upon wafer size and bridge dimensions. Each pattern 20 is representative of a bridge configuration, by way of example, and contains four piezoresistive elements to form a typical Wheatstone bridge configuration.

W. P. Maszara, in an article appearing in Vol. 138, No. 1 of the Journal of the Electrochemical Society (1991), observed that because the surface roughness of silicon increases with the thickness of an SiO_2 layer grown on it (for a given temperature), it is reasonable to expect that the oxide surface should also become rougher with the increasing thickness. Accordingly, by utilizing the thin oxide layer 18, the pre-diffusion can be performed while preserving the requisite smoothness of the device wafer surface.

In accordance with the technique of the present invention, the patterns which define the illustrative piezoresistive elements may be extremely fine line patterns, as may be implemented by diffusion, having a width of 0.1 to 1.0 mils. Such patterns can be accurately controlled due to advances made in the diffusion process, and further, the use of diffusion controls the spreading of line widths.

Referring to FIG. 5, the next step in the procedure is depicted. After formation of the degenerately doped, pattern defining regions on the wafer 10, the oxide layers 14 and 18 are removed and the N-type silicon wafer 10 is etched to reduce the thickness at the top surface. The etching is done by a conductivity selective etch. Such etches are well known, and there are etchants such as hydrazine which selectively attack the low conductivity N-type material without etching or in any manner attacking the high conductivity P+ regions. The techniques for etching silicon are well known in the art.

According to the method, the material from the N-type wafer 10 is etched away to a depth of approximately 1 micron to produce the structure shown in FIG. 5. With reference to FIG. 6, it can be seen that a layer of quartz 22, which may be on the order of 1000 to 2000 angstroms thick, is sputtered or otherwise formed on the surface of the device wafer. When referring to quartz, it is understood that silicon dioxide is equivalent. An opening 28 similar to that used in the prediffusion step is provided in the quartz layer 22 by preferential

THIS PAGE IS MISSING IN ORIGINAL DOCUMENT

providing a second semiconductor wafer having an insulating layer of a silicon compound disposed thereon;

contacting the surface of said pattern to said insulating layer; and

bonding said first and second semiconductor wafers at an elevated temperature.

2. The method according to claim 1, wherein said high conductivity pattern is diffused through a thin layer of an insulating silicon compound.

3. The method according to claim 2, further comprising the step of stripping said thin layer and re-diffusing said high conductivity pattern.

4. The method according to claim 3 wherein said stripping step is performed prior to said etching step.

5. The method according to claim 3, wherein said re-diffusing step is performed by diffusing boron into said first semiconductor wafer, thereby forming a thin layer of B_2O_3 glass over said pattern.

6. The method according to claim 1, wherein said pattern comprises a circuit pattern.

7. The method according to claim 6, wherein said circuit pattern is a piezoresistive bridge pattern.

8. The method according to claim 7, wherein said pattern is a power circuit pattern.

9. The method according to claim 6, further including the step of etching a surface of said first wafer so that said circuit pattern projects from said first semiconductor wafer.

10. The method according to claim 1, wherein said first and second wafers are bonded at said elevated temperature for less than 15 minutes.

11. A method of fabricating a piezoresistive semiconductor structure for use in a transducer comprising the steps of:

diffusing a piezoresistive pattern into a surface of a first semiconductor wafer;

etching a portion of said surface to raise said piezoresistive pattern;

providing a second semiconductor wafer having an insulating layer of a silicon compound disposed thereon;

contacting the surface of said pattern to said insulating layer; and

bonding said first and second semiconductor wafers at an elevated temperature.

12. The method according to claim 11, wherein said piezoresistive pattern is diffused through a thin insulating layer of a silicon compound of said first semiconductor wafer.

13. The method according to claim 12, further comprising the step of stripping said thin insulating layer and re-diffusing said pattern.

14. The method according to claim 13 wherein said stripping step is performed prior to said etching step.

15. The method according to claim 13, wherein said re-diffusing step is performed by diffusing boron into said first semiconductor wafer, thereby forming a thin layer of B_2O_3 glass over said piezoresistive pattern.

16. The method according to claim 10 where the elevated temperature is at as low as 900° C. to 1000° C.

* * * * *